Cell Reports
Physical Science

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Review

Emerging memory devices for neuromorphic computing in the Internet of Medical Things

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https://doi.org/10.1016/j.xcrp.2025.102735

SUMMARY

This review examines recent advances in emerging memory devices for neuromorphic computing within the Internet of Medical Things (IoMT). By integrating novel materials, brain-inspired computational architectures, and bioinspired algorithms, these technologies collectively enable efficient, adaptive, and secure biosignal processing at the edge. The review critically evaluates the strengths and limitations of devices such as resistive, ferroelectric, and photonic memories, highlighting their pivotal roles in overcoming the bottlenecks of conventional CPU/GPU-based systems. In addition, innovations in biocompatible packaging and seamless biointegration are discussed, emphasizing their potential for real-world clinical deployment. These advancements not only enhance energy efficiency, real-time processing, and miniaturization but also support the development of smarter biosensors, neural prosthetics, and wearable diagnostic platforms. The broader significance of this work lies in paving the way for next-generation, intelligent, secure, and patient-centric medical devices, thus accelerating the digital transformation of healthcare through advanced neuromorphic IoMT ecosystems.

INTRODUCTION

The Internet of Medical Things (IoMT) has rapidly emerged as a transformative paradigm within healthcare, driven by the explosive growth of wearable and implantable biomedical devices designed to enable personalized healthcare delivery.[1–4] These IoMT devices have fundamentally reshaped clinical practice and patient care through continuous, real-time physiological monitoring; proactive diagnostics; and improved therapeutic interventions, ultimately enhancing patient outcomes and healthcare efficiency. The proliferation of IoMT solutions introduces significant demands on edge computing technologies, particularly requiring advancements in real-time analytics capabilities, reduced energy consumption, and sustained, uninterrupted monitoring to facilitate patient mobility and independence.[5,6] Nevertheless, conventional computing architectures based predominantly on the classical von Neumann design face several intrinsic challenges that significantly restrict their integration into IoMT devices. First, these architectures inherently exhibit high power consumption due to intensive data movement between memory and processor units, significantly limiting battery life and thereby compromising the portability and usability of wearable and implantable medical systems.[7,8] Second, the fundamental separation of data storage and processing units, the so-called von Neumann bottleneck, introduces latency, impairing the ability of these devices to achieve the instantaneous data processing necessary for timely clinical decision-making and real-time patient interventions.[9–11] Last, conventional digital processors such as central processing units (CPUs) and graphics processing units (GPUs) face substantial hurdles in miniaturization, as their complex circuitry and thermal management requirements complicate their integration into compact, flexible, and biologically compatible medical form factors, further constraining their practical implementation in IoMT contexts.[12] Consequently, these limitations drive the pursuit of alternative computing paradigms to improve energy efficiency, reduce latency, and enhance scalability in IoMT applications.

To address these demands, neuromorphic computing has emerged as a compelling alternative paradigm explicitly designed to address intrinsic limitations associated with conventional computing architectures.[13–17] Inspired by the efficiency, adaptability, and structural complexity of biological neural systems, neuromorphic computing leverages core neural principles such as synaptic plasticity, spike-based signaling, analog information processing, and event-driven computation. These bioinspired features collectively deliver substantial improvements in computational efficiency, energy consumption, and parallel processing, making neuromorphic systems especially suitable for resource-constrained and latency-sensitive biomedical applications.[18–20] Central to the realization of neuromorphic computing are emerging non-volatile memory technologies, including resistive random-access memory (RRAM), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and other novel devices. These technologies inherently support neuromorphic implementations due to their analog switching characteristics, multilevel conductance states, intrinsic non-volatility, and

compatibility with highly parallelized architectures analogous to biological neural networks.[21–27] Among these, RRAMs are particularly notable for their ability to emulate synaptic plasticity via resistance modulation, achieving compactness, ultra-low-power consumption, and efficient analog data storage.[21,22] FeRAM and MRAM further complement RRAMs by offering rapid switching speeds, robust endurance, and reduced operational power requirements.[23,24] Additionally, emerging memory devices based on two-dimensional (2D) materials (e.g., MoS_2- and hexagonal boron nitride [hBN]-based RRAM) possess advantages such as exceptional mechanical flexibility, reduced switching energies, and excellent biocompatibility, making them highly suitable for wearable or implantable biomedical systems.[25] Similarly, perovskite-based memories leverage ion migration mechanisms to provide adaptive synaptic functionality, while optical memory devices exploit photonic mechanisms to enable ultra-fast operation, low-energy data transmission, and high-density integration, offering promising opportunities for high-speed and energy-efficient neuromorphic systems.[26,27]

To fully leverage these advantages, innovative architectural solutions like crossbar arrays have become essential, as they facilitate the effective integration of memory technologies into neuromorphic systems. Crossbar array architectures consist of 2D grids of memory elements positioned at the intersections of perpendicular conductive lines. Such crossbar arrays enable highly parallel analog computations, emulating biological neural connectivity while offering compact device size, high computational density, minimal latency, and significantly reduced energy consumption.[28–30] Crossbar architectures leverage analog conductance modulation and multilevel states of emerging memory devices to perform neural operations, such as vector-matrix multiplications (VMMs), directly within memory elements. This approach significantly alleviates the energy and latency bottlenecks inherent in conventional von Neumann architectures.[31] Consequently, memory-integrated crossbar arrays offer compelling advantages for biomedical IoMT devices, facilitating real-time physiological signal analysis, rapid detection of physiological anomalies, and sustained autonomous operation. These capabilities collectively represent a transformative advancement toward intelligent, personalized, and reliable IoMT systems, ultimately reshaping the landscape of biomedical healthcare delivery.[32,33] Despite these significant advantages, practical realization of crossbar-based neuromorphic systems with emerging memory devices in biomedical IoMT applications remains challenging. Key obstacles include device variability, integration complexity, and reliability under physiological conditions, all of which must be addressed to translate laboratory demonstrations into practical biomedical implementations.[34–36] Therefore, this review systematically investigates recent advancements and emerging trends in memory-based neuromorphic computing architectures designed for biomedical and IoMT applications. The objectives are to comprehensively evaluate existing technologies, clearly articulate prevailing implementation barriers, and highlight promising future research directions, thereby guiding the development of clinically impactful neuromorphic systems.

To provide an integrated perspective, Figure 1 summarizes the continuum from emerging memory device foundations (e.g., filamentation, phase change, ferroelectricity, and magnetooptics) through system-level crossbar array integration and toward application frontiers in biosignal analysis, neural interfacing, and intelligent IoMT platforms. The remainder of this review first provides an in-depth discussion of various emerging memory technologies, evaluating their characteristics, performance metrics, and suitability for biomedical contexts. Subsequently, crossbar array architectures and their neuromorphic computing implementations are examined, along with associated technical challenges and opportunities for improvement. The review then illustrates practical biomedical and IoMT applications to demonstrate the potential, utility, and real-world impact of neuromorphic technologies. Finally, key technological and practical barriers currently limiting widespread adoption are summarized, and a perspective on promising future research trends and directions is presented.

CLASSIFICATION AND EMERGING TECHNOLOGIES OF NON-VOLATILE MEMORY DEVICES

Resistive random-access memory

The memristor, first theorized by Leon Chua in 1970 and experimentally demonstrated by Strukov et al. in 2008, is recognized as the fourth fundamental circuit element.[40,41] These passive, two-terminal, non-volatile memory devices adopt a metal-insulator-metal (MIM) structure, as shown in Figure 2A, consisting of an active electrode, a switching layer, and a counter electrode, capped to allow interaction with the local environment (e.g., H_2O and O_2). The central switching film enables resistive modulation through electric-field-induced ion migration. Typically, memristors switch between a high-resistance state (HRS) and a low-resistance state (LRS), with some designs supporting multilevel resistance states to increase data density.[42]

Most RRAM devices rely on redox-based mechanisms: ions generated by redox reactions at the electrode diffuse through the switching medium, forming or disrupting conductive filaments. These dynamic processes governed by chemical, electrical, and mechanical interactions are key to controlling the device's resistive state and achieving reliable, scalable, and energy-efficient memory operation. This process closely resembles synaptic plasticity, namely potentiation and depression, in biological systems. Leveraging this analogy, extensive research has explored the use of RRAM in neuromorphic computing and in-memory computing (IMC) to enable massive parallelism, overcome the memory wall, and enhance energy efficiency.[49,50] Furthermore, RRAM's non-volatile nature eliminates the need for constant power to retain data, unlike static random-access memory (SRAM) or dynamic random-access memory (DRAM), significantly reducing energy consumption. These characteristics make RRAM particularly well suited to IoMT applications, which demand ultra-low power, real-time performance, and high energy efficiency.

Ferroelectric memory devices

Ferroelectric memory technologies represent a class of non-volatile memory devices that leverage the intrinsic polarization

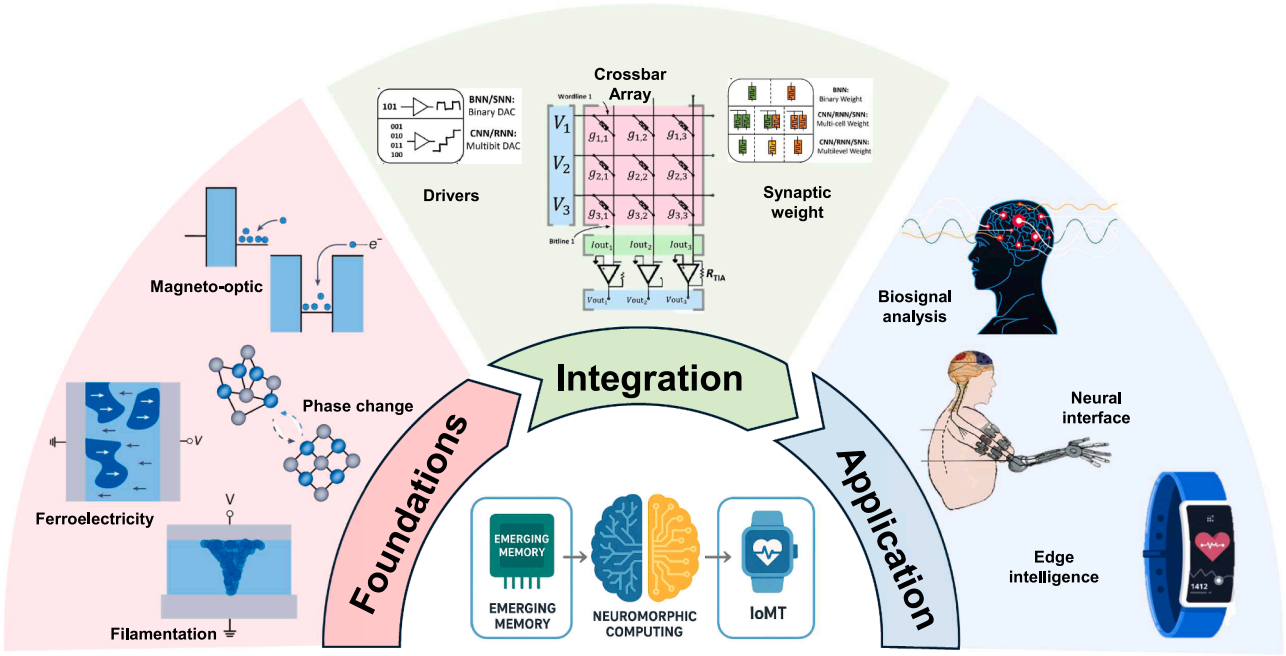

Figure 1. A conceptual overview of emerging memory-based neuromorphic biomedical systems

This figure illustrates the technological continuum from novel memory device mechanisms, such as filamentation, ferroelectricity, phase change, and magnetooptic effects, through crossbar array integration and in-memory computing architectures to translational biomedical applications. Advanced memory devices are integrated into crossbar arrays, enabling programmable synaptic weights and energy-efficient vector-matrix multiplication, which form the hardware foundation for neuromorphic computation. These integrated systems are propelling a new generation of applications in biosignal analysis, neural interfacing, and edge intelligence for the Internet of Medical Things (IoMT). The convergence of innovative materials, system-level integration, and application-driven design is paving the way for intelligent, adaptive, and miniaturized medical technologies. Figure elements are adapted from previously published works. Reproduced with permission,[37] copyright 2023, Nature; permission,[38] copyright 2022, IEEE; permission,[31] copyright 2024, Nature; and permission,[39] copyright 2023, Wiley.

properties of ferroelectric materials for information storage. As illustrated in Figure 2B, FeRAM, originally invented by Dudley Allen Buck, shares a structural similarity with DRAM, comprising a metal-oxide-semiconductor field-effect transistor (MOSFET) and a ferroelectric capacitor.[51,52] Information is stored in the form of positive or negative polarization states within the capacitor, and the read operation is destructive, necessitating subsequent data restoration. In addition, alternative ferroelectric memory topologies have been proposed, including the ferroelectric field-effect transistor (FeFET) and the ferroelectric tunnel junction (FTJ), as shown in Figures 2B and 2D, respectively.[53,54] The FeFET integrates a ferroelectric layer into the gate dielectric of a MOSFET, wherein the polarization state modulates the device threshold voltage (V_{th}). The application of positive or negative gate voltage pulses induces charge accumulation or depletion in the channel, thereby programming the transistor into high- or low-V_{th} states, which correspond to distinguishable channel current levels during readout. The FTJ, a two-terminal structure analogous to RRAM, leverages polarization-dependent modulation of tunneling resistance to encode binary states. Notably, FTJs enable non-destructive readout via resistance sensing, thereby allowing reliable and efficient memory access.

Ferroelectric memory has experienced a notable resurgence in recent years, largely driven by the discovery of ferroelectricity in scalable and complementary metal-oxide semiconductor (CMOS)-compatible hafnium oxide (HfO_2). This material breakthrough has enabled aggressive downscaling to sub-10-nm nodes while preserving key performance attributes, including ultrafast read/write speeds (20–80 ns), low write energy (~1 fJ), and high endurance exceeding 10^{10} switching cycles.[55–57] Collectively, these device architectures underscore the versatility and promise of ferroelectric memory technologies in addressing the stringent requirements of low-power, high-density, and non-volatile memory solutions for neuromorphic and biomedical computing environments.

Magnetic-based memory devices

Magnetic-based memory technologies, particularly MRAM, have garnered considerable interest due to their unique combination of non-volatility, long data retention, virtually unlimited read/write endurance, and potential for multilevel cell (MLC) operation. The core component of MRAM is the magnetic tunnel junction (MTJ), comprising two ferromagnetic layers, one with fixed magnetization and the other free to switch, separated by a thin insulating barrier.[58] The resistance state of the MTJ, determined by the relative alignment (parallel or antiparallel) of the magnetic layers, encodes binary information. Multiple generations of MRAM architectures have been developed to address evolving performance and scalability requirements. As illustrated in Figure 2E, the earliest implementation, field-driven or toggle MRAM, employs magnetic fields generated by orthogonal write lines to toggle the free layer's magnetization. Despite

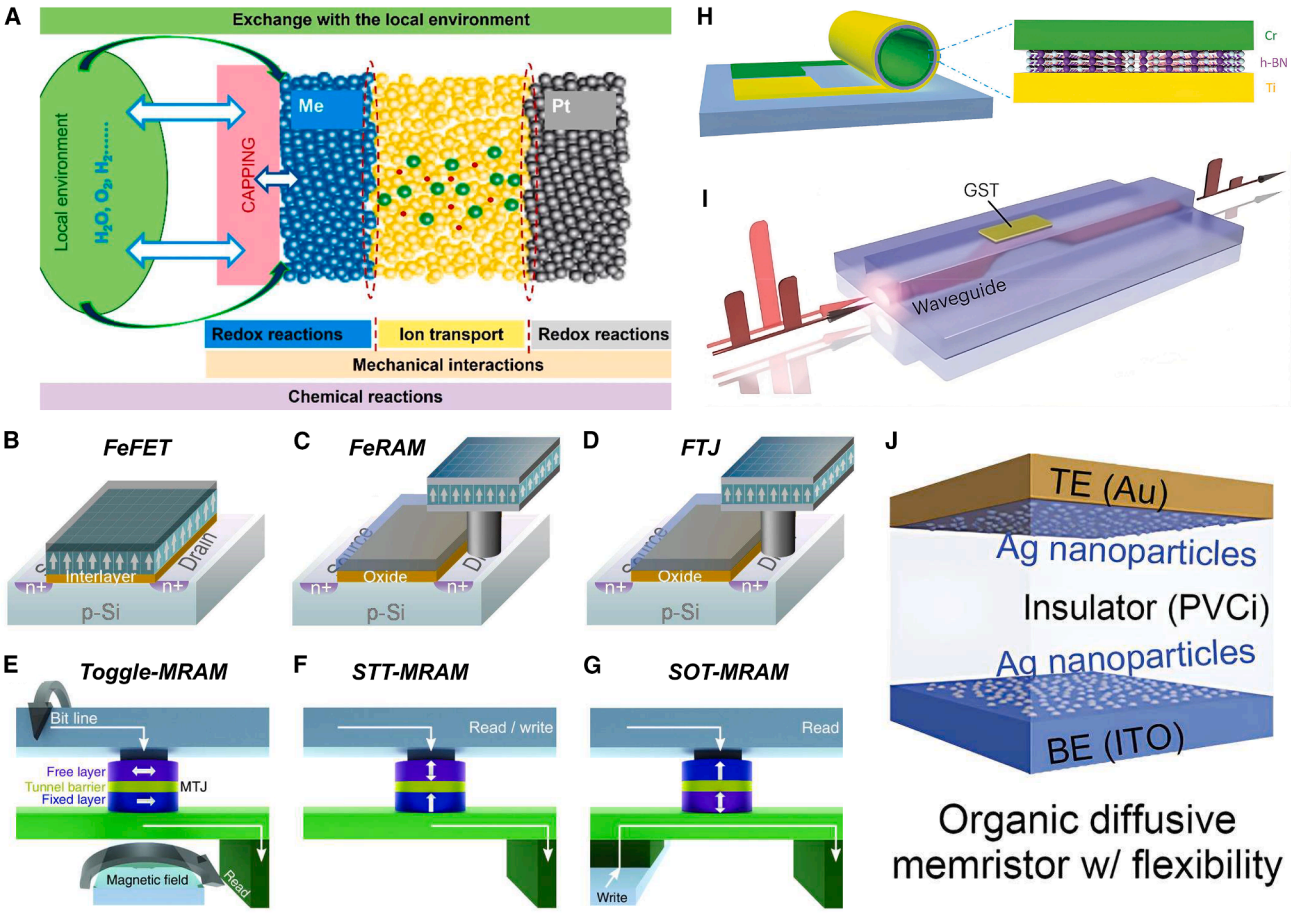

Figure 2. Overview of emerging non-volatile memory devices

(A) Schematic of a redox-based memristive device structure, illustrating the electrochemical metallization process. Reproduced with permission.[43] Copyright 2023, ACS.

(B–D) Three structures of ferroelectric memory devices: (B) FeFETs incorporate ferroelectric materials into the gate of a field-effect transistor, using polarization to regulate channel electrons and thereby realize distinct low-V_{th} and high-V_{th} states. (C) FeRAMs employ a one-transistor, one-capacitor (1T1C) cell structure. (D) FTJ with a one transistor, one resistor (1T1R) structure. Reproduced with permission.[44] Copyright 2021, ACM.

(E–G) Three structures of MRAM architecture: (E) toggle-MRAM leverages magnetic fields to flip the magnetization state of its magnetic tunnel junction (MTJ). (F) STT-MRAMs let an electric current directly through an MTJ to write their cells. (G) SOT-MRAM has an electric current flow through the write line, which generates magnetic torques to flip the MTJ. Reproduced with permission.[45] Copyright 2022, Wiley.

(H) A rolled-up hexagonal-BN tube fabricated on an SiO_2 substrate showing the flexibility of a 2D-material memristor. Reproduced with permission.[46] Copyright 2019, Wiley.

(I) Optical memory cell made of $Ge_2Sb_2Te_5$ (GST), whose state is written and read through optical pulses. Reproduced with permission.[47] Copyright 2015, Nature.

(J) The device architecture of the polymer-based organic memristor. Reproduced with permission.[48] Copyright 2023, Wiley.

its functional viability, this architecture suffers from scalability limitations, including high write current demands (up to 80 mA at 30 ns), excessive energy consumption, and the half-select issue.[59]

To mitigate these drawbacks, spin-transfer torque MRAM (STT-MRAM), shown in Figure 2F, was introduced.[60,61] STT-MRAM achieves magnetization switching by injecting a spin-polarized current vertically through the MTJ, enabling lower power operation and improved scalability. This architecture is well suited to embedded applications, particularly as a replacement for embedded flash (eFlash) in microcontrollers. In addition, due to their spin-dependent mechanisms, STT memristors offer a promising platform for storing and manipulating quantum spin states with high endurance and low noise.[62,63] However, STT-MRAM is constrained by several issues, such as a limited on/off resistance ratio, which increases the read error rate; trade-offs between write current density and thermal stability; and integration challenges arising from its complex multilayer stack.

To address these challenges and further enhance performance, spin-orbit torque MRAM (SOT-MRAM) has emerged as a promising next-generation solution, as depicted in Figure 2G.[64] In this architecture, the write current flows laterally through a heavy-metal underlayer, generating a spin current via the spin Hall effect that switches the free layer magnetization. Importantly, the separation of read and write paths eliminates read

disturbance and improves data retention reliability. SOT-MRAM offers sub-nanosecond switching speeds and significantly reduced write currents (on the order of 500 μA), making it ideal for high-speed, non-volatile applications such as L1 caches, while retaining the energy efficiency and endurance necessary for IoMT platforms.[65]

Emerging memory technologies

Resistive memory devices incorporating 2D materials have emerged as promising candidates for next-generation neuromorphic systems. As illustrated in Figure 2H, these devices typically adopt a vertical architecture, in which stacked layers of 2D materials, such as MoS_2, WS_2, and hBN, are sandwiched between two flexible electrodes.[66–68] The atomically thin structure significantly reduces the operating voltage (as low as 0.1 V) and enables exceptionally high on/off current ratios, often exceeding 10^{11}.[69] The weak van der Waals bonding between adjacent layers not only facilitates the migration of ionic species necessary for resistive switching but also imparts intrinsic mechanical flexibility. This property is particularly advantageous for conformal integration into wearable and implantable biomedical systems. Furthermore, 2D-material-based memristors exhibit ultra-fast switching speeds (120 ps) and ultra-low power and energy consumption, with reported values as low as 1 fW and 8.8 zJ, respectively.[70,71] These characteristics position 2D memristors as highly suitable for energy-efficient, high-speed memory applications in resource-constrained neuromorphic computing platforms.

Perovskite materials, typically expressed with the formula ABX_3 (where A and B are cations and X is an anion), such as $CaTiO_3$, $MAPbI_3$, and $LaFeO_3$, offer a highly tunable crystal structure that enables a wide spectrum of electrical functionalities, including semiconducting, insulating, superconducting, ferroelectric, and multiferroic behaviors.[72] This tunability makes them promising candidates for next-generation memristive devices. In particular, halide perovskites like $MAPbI_3$ exhibit fast ion migration and low activation energy barriers, facilitating efficient resistive switching with low write voltages (~0.1 V) and high on/off resistance ratios (up to 10^6).[73–75] These devices can be processed at low temperatures (100°C–110°C) and integrated on flexible substrates, supporting the development of lightweight, stretchable, and wearable neuromorphic systems. Some perovskite memristors also demonstrate multilevel conductance states, enabling analog-like synaptic behavior.[76] However, challenges remain: their operational stability is often compromised by sensitivity to moisture, heat, and mechanical stress, and current device structures offer limited data retention time (~10^5 s) and endurance (~10^4 mechanical cycles). The data will be lost longer than this retention time or bent more than the above mechanical cycles.[77] Moreover, their poor compatibility with standard CMOS technology hinders large-scale production.

Phase-change materials (PCMs) have long been employed as the storage medium in optical data storage systems such as compact disks (CDs). However, despite utilizing photonic carriers for data retrieval, data access and computation in these systems remain confined to the electronic domain. Moreover, the switching process between crystalline and amorphous states requires inefficient joule-level thermal energy. In contrast, recently developed optical memory technologies, particularly all-photonic memories and optical memristors, as shown in Figure 2I, offer a promising alternative by enabling fully photonic data storage and transmission.[47] These devices offer exceptionally high data rates, reaching up to 10–20 Gb/s for both read and write operations, along with significantly reduced power consumption.[78,79] By employing wavelength-division multiplexing (WDM), multiple data streams can be processed in parallel, enabling ultra-high memory bandwidth. Advanced implementations based on InP/InGaAsP photonic integrated circuits have achieved ultra-fast switching times as low as 20 ps with minimal optical switching energy (~5.5 fJ), highlighting their promise for high-speed, energy-efficient neuromorphic and in-memory computing applications in biomedical and IoMT systems.[80]

Organic memristors employ organic materials such as polymers, metal-organic frameworks, covalent- and hydrogen-bonded frameworks, and carbon-based compounds as active layers for resistive switching.[81–83] Their operation is based on the formation and rupture of conductive filaments within the organic matrix. These devices support low-cost, solution-based fabrication like spin coating, allowing large-area, low-temperature, and scalable production. Unlike inorganic counterparts, organic memristors offer mechanical flexibility and biocompatibility, making them ideal for flexible neuromorphic electronics and wearable biomedical systems. Some devices operate at ultra-low voltages down to 0.3 V and switching energies as low as 39.56 nW.[84,85] However, reliability remains a challenge. Retention time is limited to about 100,000 s.[86] The highest reported number of endurance cycles is 10^6 with a low operation speed (340 μs).[87] Environmental sensitivity, particularly to humidity, also hinders long-term performance. Ongoing efforts in material engineering and encapsulation are critical to improve stability and unlock the potential of organic memristors for biomedical IoMT applications.

Comparative evaluation of device characteristics

To address the stringent demands of biomedical Internet of Things (IoT) applications, memory technologies must fulfill several critical requirements. First, non-volatility combined with high endurance and long retention time is essential for continuous physiological monitoring and reliable long-term data storage, particularly in devices with limited communication bandwidth or intermittent power supply.[88,89] Second, low switching energy, moderate access latency, and minimal programming voltages are vital for achieving energy-efficient operation in battery-constrained environments.[90] Third, CMOS compatibility and in-memory computing capabilities enable seamless integration with neuromorphic architectures, minimizing data movement and supporting low-power, real-time edge analytics—particularly valuable for anomaly detection in biomedical signals.[91] Last, mechanical flexibility and robustness under deformation are imperative for ensuring stable performance in wearable and implantable biomedical devices.[92]

In Table 1, we compare mainstream memory technologies, such as RRAM, FeRAM, MRAM, photonic memory, and organic memristor, regarding the requirements posed by the biomedical IoT above. Among RRAM technologies, redox-based RRAM stands out with its mature fabrication process, offering a favorable balance of power consumption, operational speed, and

Table 1. Comparative analysis of emerging non-volatile memory technologies: RRAM, ferroelectric memory, MRAM, and photonic memory

Class	Device	Material	Write voltage	Read voltage	Switch energy	Read time	Write time	On/off ratio	Endurance	Retention	Flexibility
RRAM	redox RRAM[96]	HfZnO	0.95–1.05 V	<0.2 V	19 pJ	–	30 ns	>10	10^5 cycles	>10 years	no
	perovskite RRAM[97]	$MAPbI_3$	2.2–2.4 V	0.15 V	–	100 ps	100 ps	10^7	$\sim10^6$ cycles	>2 years	yes
	2D RRAM[61]	hBN	2.25–2.75 V	0.5 V	2 pJ	120 ps	120 ps	–	600 cycles	10 years	yes
	organic memristor[98]	DNA/Ag NPs	0.2–0.3V	–	–	–	20 ns	10^6	1,000 cycles	10^5 s	yes
Ferroelectric memory	FeRAM[47]	HfO_2	1.5–3.5 V	0.5 V	–	50 ns	50 ns	–	10^{10} cycles	10 years	no
	FeFET[99]	$Hf_{0.5}Zr_{0.5}O_2$	4.2 V	1.4 V	–	100 ns	100 ns	2×10^4	10^6 cycles	10 years	no
	FTJ[100]	PZT	5 V	0.05 V	5.3 fJ	630 ps	630 ps	~200	10^9 cycles	10^4 s	no
MRAM	STT-MRAM[101]	MgO	0.72–0.88 V	0.6 μA	–	6 ns	100 ns	–	10^6 cycles	20 years	no
	SOT-MRAM[102]	MgO	1.6 V	1.4 V	–	15 ns	5 ns	–	10^{10} cycles	10 years	no
Photonic	photonic memory[103]	Ce:YIG	21.5 mV	–	2.28 pJ	1 ns	1 ns	–	2.4×10^9 cycles	>4 days	no

Lead zirconate titanate, PZT.

endurance. It has already been adopted in numerous in-memory computing designs, making it a promising non-volatile memory candidate for low-power biomedical IoT systems.[49,50,93] In contrast, emerging RRAM devices based on perovskite, organic, and 2D materials offer unique mechanical flexibility, rendering them particularly suitable for conformable or implantable sensors with integrated computation. These devices operate at low voltages and demonstrate ultra-fast switching speeds, which are advantageous for real-time biosignal processing. However, these devices still face significant challenges. Specifically, 2D-material-based RRAM and organic memristors suffer from relatively low endurance, with typical lifespans of around 600 and 1,000 cycles, respectively. Additionally, perovskite RRAM and organic memristors offer only moderate data retention, approximately 2 years and 10,000 s, respectively, which limits their suitability for long-term deployment. Ferroelectric memory devices also show promise. FTJs are particularly notable for their low read voltages (0.05 V) and rapid access times (630 ps), although their short data retention (~3 h) confines their utility for short-term caching applications in ultra-low-power neuromorphic computing systems. FeRAM and FeFET offer a better trade-off, with high endurance (10 years), moderate read/write speeds (50–100 ns), and reasonable power requirements, making them suitable for IoT nodes deployed outside the human body and for performing frequent sensor data processing. Magnetic RAM (MRAM), especially in its STT and SOT variants, provides long data retention (20 years), high endurance (10^{10} cycles), and acceptable energy efficiency, which positions it as an attractive replacement for embedded flash in low-power microcontroller units used in biomedical IoT applications.[94] Finally, photonic memory delivers exceptional speed, energy efficiency, and endurance due to its light-based data handling. Nevertheless, the need for complex optoelectronic interfaces currently limits its scalability and integration in resource-constrained medical and wearable devices.[95]

Conventional CMOS memory technologies include volatile SRAM and DRAM, as well as non-volatile flash. Compared to these, the emerging memory devices summarized in Table 1 offer several compelling advantages for neuromorphic computing in IoMT applications. Although SRAM and DRAM provide fast access speeds, their volatile nature requires continuous power supply, resulting in high standby energy consumption. This makes them unsuitable for power-constrained biomedical systems. Flash, while non-volatile, suffers from limited endurance (10^4 to 10^5 cycles), high programming voltages, and relatively slow write speeds, which limit its effectiveness for real-time sensing and computing tasks.[104] In contrast, emerging memories such as redox-based RRAM, SOT-MRAM, and FeRAM combine non-volatility with low switching energy, long retention time, and high CMOS integration density. These features make them highly suitable for energy-efficient and stable data storage in IoMT applications. Moreover, in-memory computing systems built on these devices can achieve lower power consumption and higher integration density compared to those based on SRAM. Devices based on 2D materials, organics, or perovskites further offer mechanical flexibility, enabling seamless integration into conformable, wearable, or implantable biomedical platforms. Taken together, these characteristics establish emerging memory technologies as superior alternatives to conventional CMOS memories for implementing low-power, adaptive, and robust neuromorphic processing in next-generation IoMT systems.

NEUROMORPHIC COMPUTING IMPLEMENTATIONS USING CROSSBAR ARRAYS

Crossbar array structure and operating principles

A crossbar array is a 2D, grid-like architecture specifically designed for simultaneous data storage and computation. Structurally, it consists of horizontally oriented word lines intersecting vertically oriented bit lines. At each intersection point, a memory device is strategically placed, creating highly parallel storage and computation units, as illustrated in Figure 3A. The fundamental operational principle involves applying input signals, typically in the form of voltage pulses, onto the word lines. Each

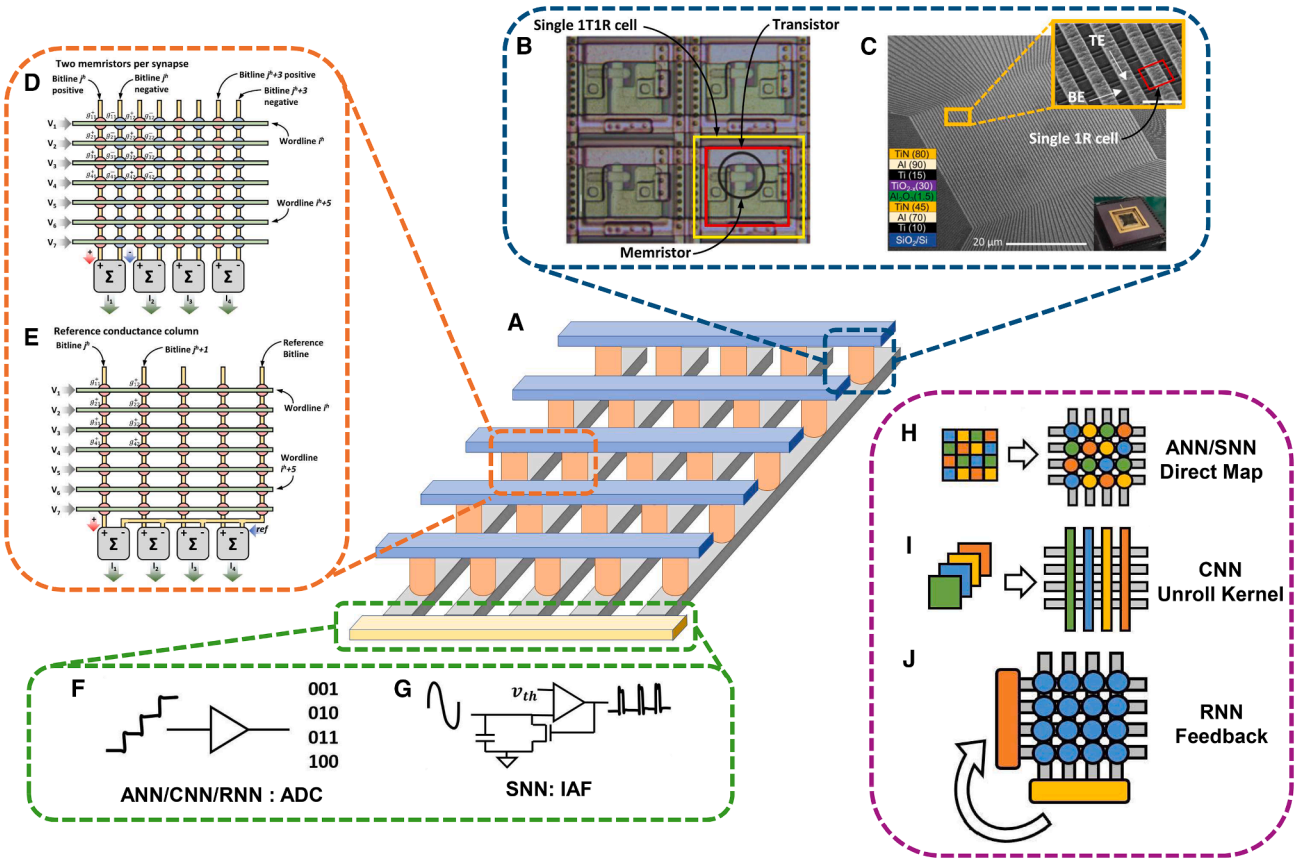

Figure 3. Schematic illustration of memristor-based crossbar array architectures and their hardware mapping for neuromorphic computing

(A) The general structure of a memristor crossbar array, which enables parallel vector-matrix multiplication for efficient in-memory computing.

(B–J) (B) Optical image of a single 1T1R (one transistor, one resistor) cell and (C) scanning electron microscope image of a single 1R (one resistor) cell, representing common integration schemes for crossbar arrays. Reproduced with permission,[106] copyright 2021, Nature; permission,[107] copyright 2018, Nature. (D and E) Different hardware encoding schemes for synaptic weights: (D) uses two memristors per synapse for differential representation of positive and negative weights, while (E) employs a reference conductance column for offset-based encoding. Reproduced with permission,[31] copyright 2024, Nature. (F and G) Peripheral circuits for neural signal processing, where (F) shows the use of analog-to-digital conversion for ANN, convolutional neural network (CNN), and recurrent neural network (RNN) models and (G) depicts an integrate-and-fire (IAF) neuron model for spiking neural networks (SNNs). Reproduced with permission,[38] copyright 2022, IEEE. (H–J) Examples of hardware mapping strategies for different neural network architectures: (H) direct mapping for ANNs/SNNs, (I) kernel unrolling for CNNs, and (J) recurrent feedback implementation for RNNs. Reproduced with permission,[38] copyright 2022, IEEE.

memory element at these intersections then responds by generating an electric current whose magnitude depends on the internal state of the device. These generated currents subsequently merge and aggregate along the bit lines, effectively executing VMM operations intrinsically. In this operation, components of an input vector are individually multiplied by corresponding "weights" stored at each intersection, with results cumulatively summed along the bit lines.[105]

One of the most compelling advantages derived from the structural and operational characteristics of crossbar arrays is their exceptional capability for massive parallelism. Given that every word line can be activated simultaneously, an $M\times N$ crossbar array can perform $M \times N$ multiply-accumulate operations concurrently within a single clock cycle. Mathematically, the readout operation of memory-based crossbar arrays can be approximated using linear ohmic relationships as follows:

$$I_j = \sum_{i=1}^{M} G(x_{i,j}) \cdot V_i \qquad \text{(Equation 1)}$$

where i and j represent the i^{th} row and j^{th} column, respectively, and $G(x_{i,j})$ represents the function of the device state at intersection (i,j), directly reflecting its internal state parameter $x_{i,j}$. This internal parameter varies significantly depending on the specific memory technology used. For instance, it may correspond to conductance states in RRAM, polarization orientations in FeRAM, or optical reflectance levels and trap state configurations in optical memristors, among others.[108–110]

This feature starkly contrasts with the sequential data processing approach in conventional von Neumann computing architectures, which inherently introduces performance bottlenecks due to the separate processing and memory units. Moreover, the innovative architecture of crossbar arrays

inherently integrates both data storage and computational functions within a single physical unit, thus effectively addressing the "memory wall" challenge encountered in traditional computing systems. This memory wall refers to the significant latency and energy overhead resulting from frequent data transfers between separate memory and processing components.[111] Recent studies have shown that the intrinsic parallelism and analog in-memory computing of crossbar arrays greatly improve neural network efficiency, especially for real-time multiply-accumulate operations.[112] This makes them highly suitable for battery-powered IoMT devices, which require continuous AI processing under tight energy constraints. Operating in the milliwatt to microwatt range, crossbar arrays enable real-time health monitoring and intervention with minimal power consumption. Their energy efficiency has been repeatedly validated, highlighting their promise for next-generation edge AI in biomedical applications.[113]

Neuromorphic computing realization

Synapses lie at the core of memory-based neuromorphic computing systems, physically realized through emerging memory devices that emulate synaptic weights. These systems utilize diverse memory cell architectures, including 1R (one resistor) and 1T1R (one transistor and one resistor) configurations, as shown in Figures 3B and 3C, respectively.[106] The 1R structure provides maximum integration density but suffers from severe sneak-path currents, which compromise array scalability and reliability. To overcome this, 1T1R cells incorporate transistors to isolate individual cells, offering improved control at the cost of increased area and fabrication complexity.[107] Representing negative weights in analog crossbar arrays presents another challenge, as most memristive devices encode only positive conductance values. A common solution is the differential pair approach in Figure 3D, where two cells represent the positive and negative components of a weight:

$$w_{i,j} = G_{i,j}^{+} - G_{i,j}^{-} \quad \text{(Equation 2)}$$

where $w_{i,j}$ represents the synaptic weight located at the intersection of the i^{th} row and j^{th} column of the synaptic weight array, $G_{i,j}^{+}$ is the conductance of the positive component, and $G_{i,j}^{-}$ is the conductance of the negative component. This method offers high precision but reduces memory density and increases wiring overhead.[31] An alternative method in Figure 3E uses a reference column, where each synaptic weight is represented as a deviation from baseline conductance:

$$w_{i,j} = G_{i,j} - G_{ref} \quad \text{(Equation 3)}$$

where $G_{i,j}$ is the actual conductance value at the crosspoint and G_{ref} is the conductance of a reference column representing the baseline or "zero" weight. While this approach maintains integration density, it demands careful calibration and is sensitive to process variations and noise, potentially degrading accuracy.[31]

Neuron dynamics in neuromorphic systems are emulated through either statistical or biophysically inspired circuit models. Statistical models, such as artificial neural networks (ANNs), convolutional neural networks (CNNs), and recurrent neural networks (RNNs), simulate layered interconnections and non-linear activation functions through deterministic training algorithms like backpropagation. These models require peripheral circuits, including transimpedance amplifiers (TIAs) and analog-to-digital converters (ADCs) shown in Figure 3F, to convert the analog output of VMM into digital signals.[114] Biophysically inspired models, primarily represented by spiking neural networks (SNNs), more closely mimic the dynamics of biological neurons by encoding information in asynchronous spike trains. Crossbar-based SNNs employ integrate-and-fire (IAF) circuits as shown in Figure 3G to transform post-synaptic currents into voltage spikes, facilitating spike-timing-dependent plasticity (STDP) learning mechanisms. Peripheral circuit enhancements, including current-stabilizing amplifiers and non-linear spiking buffers, have been proposed to ensure signal integrity and expand computational expressiveness.[115]

Mapping neural networks onto crossbars requires architecture-specific strategies. For ANNs, weight matrices are directly mapped to conductance states shown in Figure 3H, while input vectors are applied as voltages across word lines.[106] For CNNs, kernel tensors are unrolled into one-dimensional (1D) vectors and distributed across multiple crossbar columns, shown in Figure 3I, often using dual-array differentials to handle positive and negative weights. Feature maps are then sequentially input, with computational speed improved by duplicating kernel arrays for parallelization.[116] Crossbar-based implementations support ANN and CNN models with high throughput and computational density, making them effective for image processing and diagnostics in IoMT scenarios.[38] SNNs encode inputs as pulses or pulse-width-modulated signals, with IAF circuits converting integrated currents into spikes, supporting asynchronous computation and temporal coding.[115] These event-driven systems offer ultra-low power consumption and inherent robustness to variability and noise, rendering them ideal for energy-constrained, real-time monitoring tasks in IoMT devices.[117] For RNNs, recurrent feedback loops and time-gated operations are realized through staged crossbars and feedback buffers, shown in Figure 3J, forming compact neuromorphic temporal processors. Advanced architectures utilize pipelined crossbar VMM and peripheral logic to execute sequential data flows, while memristor-based long short-term memory (LSTM) circuits with *in situ* learning have been demonstrated to support real-time adaptive learning for biomedical time-series analysis.[118]

Recent advancements extend crossbar neuromorphic computing to transformer-based models. ReTransformer, for instance, implements attention mechanisms via resistive random-access memory (ReRAM)-based computing-in-memory architectures, efficiently supporting long-range temporal dependencies in biomedical time-series analysis.[119] Furthermore, memristor crossbars have enabled new applications such as Generative Adversarial Network acceleration with pipelined analog-digital blocks and reinforcement learning with analog synaptic updates.[120,121] These developments underline the versatility of memristor-based crossbars in supporting diverse machine learning paradigms for edge healthcare systems.

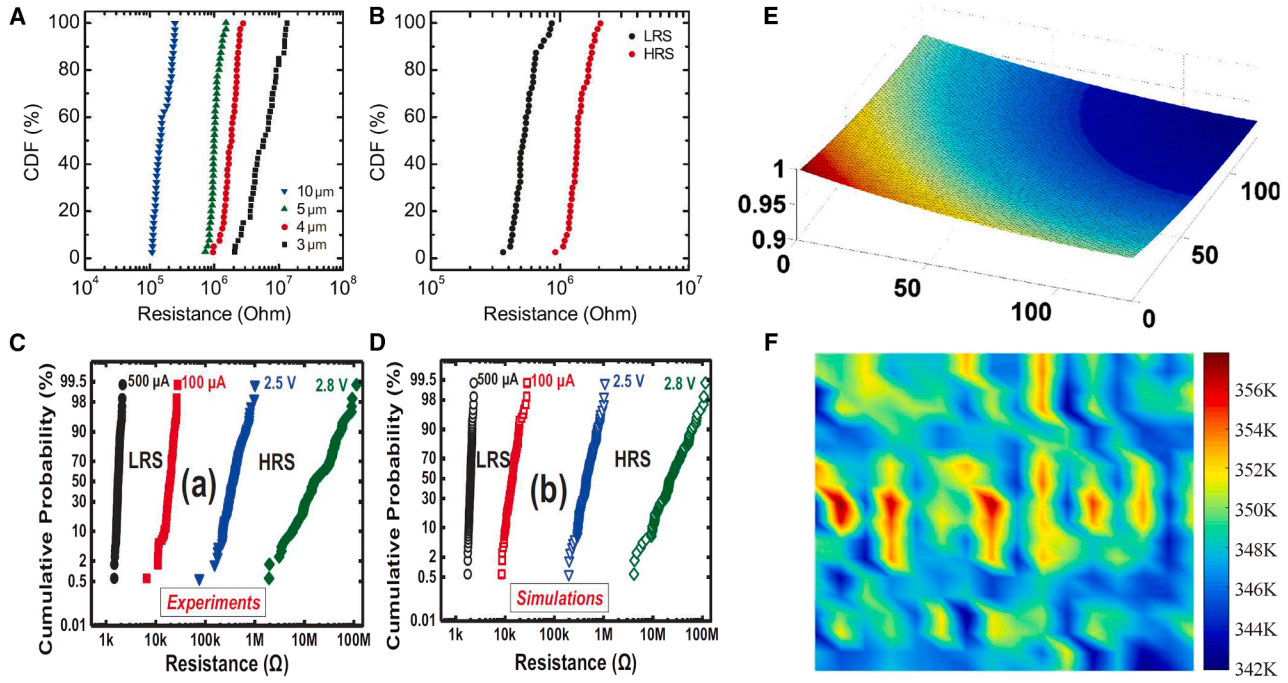

Figure 4. Device variability and reliability bottlenecks in large-scale ReRAM (memristor) crossbar arrays for neuromorphic and in-memory computing

(A and B) Cumulative distribution function (CDF) of bulk RRAM resistance: (A) shows device-to-device (D2D) variations in the pristine state across different device sizes, while (B) presents the CDFs of programmed low-resistance state (LRS) and high-resistance state (HRS) from DC sweeps in 5-μm bulk RRAM devices. Reproduced with permission.[122] Copyright 2024, Nature.

(C and D) (C) Measured and (D) simulated multilevel cell (MLC) characteristics of RRAMs, revealing significant cycle-to-cycle (C2C) resistance variations in both LRS and HRS states, which directly impact the stability of analog weight storage in crossbar neural arrays. Reproduced with permission.[123] Copyright 2015, EDAA.

(E) Three-dimensional mapping of programming voltage drop across a large crossbar array, highlighting severe IR drop at array edges due to wire and cell resistance, which degrades programming accuracy and limits scalability. Reproduced with permission.[128] Copyright 2014, IEEE.

(F) Simulated temperature distribution across a ReRAM array under high-throughput operation, showing localized thermal gradients that can accelerate device degradation and lead to inference errors if not mitigated. Reproduced with permission.[129] Copyright 2020, ACM.

Challenges and opportunities in crossbar arrays

Even if crossbar arrays hold immense promise in IoMT deployments, a series of critical reliability challenges must be resolved to ensure their practical viability. These challenges span device-level stochasticity, array-scale parasitics, and environmental variability, which cumulatively degrade computational reliability and endurance.[34]

One prominent challenge is the intrinsic variability in memristor devices, arising from both device-to-device (D2D) (Figures 4A and 4B) and cycle-to-cycle (C2C) (Figures 4C and 4D) fluctuations.[122,123] Variability in switching thresholds, conductance states, and write noise can distort synaptic weight representation and introduce significant errors in VMM operations.[124] Moreover, MLC operation, which is often employed to reduce area cost, increases vulnerability to noise and variability, especially in higher-significance bits.[125] These stochastic characteristics require advanced mitigation strategies. Algorithmically, fault-aware retraining and profiling-based compensation techniques are widely adopted.[124] On the circuit level, designs such as redundancy columns and closed-loop feedback tuning have proven effective.[126] Additionally, process variation and aging-induced drift further reduce conductance stability, prompting innovations like bipartite mapping to avoid high-variation cells and self-healing weight allocation.[127]

As array sizes grow, IR drop, which is the amount of voltage drop that occurs naturally as electric current flows through wires, becomes non-negligible.[16] Due to wire resistances in crossbars, voltage drops across bit and word lines cause unequal biasing of memristor cells, leading to weight mismatches between the target and the programmed state, as shown in Figure 4E. Techniques like 1D decomposition of weight matrices into smaller blocks and dynamic IR-drop compensation offer practical solutions.[124] These methods are increasingly integrated with simulation frameworks to assess architectural robustness under realistic conditions.[130]

Environmental conditions such as temperature fluctuations exacerbate these issues. Thermal noise and ambient heating can cause drift in programmed states and amplify variability across arrays, as shown in Figure 4F. Hardware-level countermeasures include on-chip thermal sensing, differential sensing strategies, and thermally aware layout optimization frameworks, which reduce thermal gradient-induced mismatches.[129]

Taken together, these reliability issues underscore the importance of integrated material-device-architecture-algorithm

co-design. Advancements in memristor materials promise improved retention, reduced switching variability, and higher endurance. Simultaneously, circuit-level redundancy, fault-tolerant network training, and architectural innovations such as localized routing and weight-aware mapping continue to advance the frontier of resilient memristor-based computing. Looking forward, enhancing reliability will be essential for the deployment of crossbar-based neuromorphic systems in biomedical applications, where accuracy, continuity, and energy efficiency are critical. By integrating advanced memory architectures, bioinspired learning, and optimized algorithm-hardware co-design, crossbar arrays offer a versatile and scalable solution to meet the stringent demands of next-generation IoMT technologies.

NEUROMORPHIC COMPUTING IN BIOMEDICAL ENGINEERING AND IoMT APPLICATION

Overview

The convergence of memristive and neuromorphic technologies with biomedical engineering is enabling compact, low-power systems capable of real-time, adaptive processing directly at the point of care.[131] Unlike conventional architectures that separate memory, computation, and sensing, memristive platforms integrate these functions into unified physical substrates, allowing for efficient biosignal interpretation, neural interfacing, and secure edge intelligence. These capabilities are particularly crucial within the IoMT, where decentralized, responsive, and privacy-preserving operation forms the foundation of clinically viable systems.[132] Decentralization allows local, on-device processing that reduces latency and enhances system autonomy, which is essential for real-time physiological monitoring and intervention. Responsiveness ensures that rapidly changing biosignals can trigger timely feedback or control actions, critical in closed-loop scenarios such as cardiac monitoring or neural modulation. At the same time, privacy-preserving mechanisms are vital for protecting sensitive health data, especially as many IoMT devices operate in uncontrolled environments and are vulnerable to security breaches. As the field matures, attention is shifting from device-level proofs of concept to application-driven system integration, where reliability, scalability, and long-term adaptability will determine the translational success of memristive biomedical technologies. These developments point toward a new generation of intelligent, integrated, and secure medical systems capable of transforming human-machine interaction in healthcare.

On-device biosignal analysis

Memristive neuromorphic platforms are redefining biosignal analysis by enabling real-time, in-memory computation that inherently mirrors the spatiotemporal complexity of biological signals. In contrast to conventional von Neumann architectures that separate memory and processing, memristor-based systems unify the two functions, allowing direct encoding and interpretation of dynamic biosignals with minimal energy and latency overhead. This architectural paradigm is particularly advantageous for wearable and implantable health monitoring, where local, low-power computation is essential for continuous operation without reliance on cloud resources. Jiang et al. demonstrated this capability through the Memristor-Spiking Processing and Adaptive Network (MSPAN), an event-driven electrocardiogram (ECG) classification engine that integrates adaptive spiking neurons with memristive synapses.[133] The system achieved 93.6% classification accuracy with just 0.52 ms latency and 0.178 μJ energy consumption per heartbeat, significantly surpassing conventional LSTM and CNN models in both responsiveness and power efficiency. Such performance makes it suitable for closed-loop cardiac monitoring applications where real-time feedback is critical. Expanding this concept to flexible and deformable electronics, Lee et al. developed a self-rectifying memristive array based on flexible memristive dot product engine (f-MDPE), designed for biosignal classification on skin-mountable substrates, as shown in Figure 5A.[134] Their architecture delivered sub-millisecond inference at just 120 nJ per decision, over 300× more efficient than CPU or GPU baselines while preserving high classification accuracy under mechanical strain. These advancements collectively highlight the feasibility of integrating neuromorphic intelligence directly into edge biosensors, laying the foundation for autonomous, wearable diagnostic systems capable of operating continuously and intelligently in real-world physiological environments.

Adaptive physiological monitoring

Recent innovations have extended biosignal analysis beyond static classification to dynamic modeling of physiological processes, reflecting a growing demand for continuous, context-aware health monitoring. Unlike traditional systems that rely on snapshot-based decision-making, adaptive neuromorphic models aim to capture the evolving nature of biosignals such as electroencephalogram (EEG), eye movement, and respiration, enabling more accurate interpretation of physiological states over time. Reservoir computing, a recurrent neural architecture particularly suited to processing time-varying signals, has found renewed relevance through its hardware realization on memristive substrates. Yuan et al. demonstrated a biomemristor-based reservoir computing system enhanced with a multivalued masking mechanism, which increased the temporal richness and separability of EEG signal representations.[136] By leveraging analog conductance dynamics and the fading memory effect intrinsic to memristors, the system was able to extract fine-grained spatiotemporal features without requiring complex preprocessing pipelines. Building on this, Cai et al. proposed a heterogeneous memristive platform that performs vector-matrix operations across multiple neuromorphic paradigms, including spiking, recurrent, and convolutional models.[137] This platform enabled biometric authentication and eye-movement decoding under real-world, time-varying, multimodal input conditions. These advances mark a paradigm shift from static, task-specific inference to continuous, adaptive signal understanding. By embedding learning, memory, and signal transformation directly into the hardware, memristive neuromorphic systems offer unprecedented potential for *in situ* physiological monitoring. This is particularly relevant for wearable and implantable devices, where the ability to track, learn from, and respond to dynamic physiological rhythms in real time is essential for personalized, autonomous healthcare.

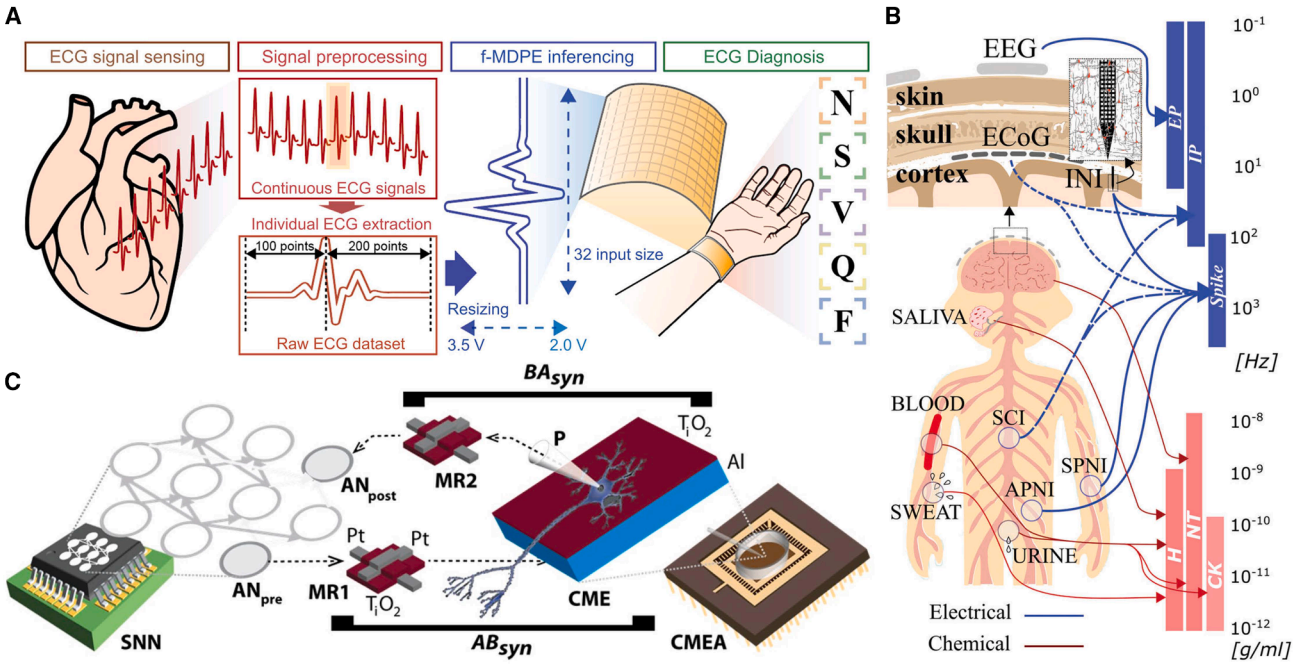

Figure 5. Schematic illustration of bioelectronic and neural interfaces for biosignal processing and diagnosis

(A) Workflow for biosignal-based disease diagnostics using a neuromorphic system. The pipeline includes ECG signal sensing, signal preprocessing, feature extraction through f-MDPE (flexible memristive dot product engine), and ECG diagnosis into specific arrhythmia classes (N, S, V, Q, and F). Reproduced with permission.[134] Copyright 2025, Nature.

(B) Electrical and chemical signals detected in the human body. Brain signals are measured via EEG (extracranial), electrocorticography (ECoG) (cortical surface), or implanted neural interfaces (INI; intracortical). Signals can also be recorded from the spinal cord (SCI) and peripheral nerves—somatic (SPNI) or autonomic (APNI). Recordings reflect changes in electrical potentials, evoked potential (EP) (EEG) and IP (ECoG and INI), capturing local field potentials (LFPs) and single-neuron spikes. Blue bars indicate signal bandwidths. Body fluids carry biomarkers like neurotransmitters (NTs), hormones, and cytokines (CKs); red bars show typical concentration ranges. Reproduced with permission.[39] Copyright 2023, Wiley.

(C) Diagram of the hybrid circuit and synaptors. AN_{pre} and AN_{post} are silicon spiking neurons in a very-large-scale integration SNN; MR1 and MR2 are Pt/TiOx/Pt memristors. Rat hippocampal neurons grow on a TiO_2-coated multielectrode array (CMEA) with a capacitive electrode (CME). A patch-clamp pipette (P) records from one neuron (BN). Synaptors AB_{syn} and BA_{syn} link $AN_{pre} \rightarrow$ BN and BN $\rightarrow AN_{post}$. Memristors mimic synaptic plasticity, while CME and P enable bidirectional signal transfer between electronics and the biological neuron. Reproduced with permission.[135] Copyright 2020, Nature.

Flexible bioelectronics

Realizing neuromorphic intelligence in real-world biomedical environments demands systems that not only emulate brain-like computation but also integrate seamlessly with soft, dynamic biological tissues. Flexible and biocompatible memristive platforms address this challenge by offering mechanically adaptive architectures capable of conforming to physiological surfaces without compromising electronic performance. Mao et al. reviewed a class of biomemristor-integrated systems embedded in textile electronics and skin-mountable substrates, demonstrating stable switching behavior under mechanical deformation, which is an essential attribute for continuous operation in wearable and prosthetic applications.[138] These devices maintained electrical integrity under tensile strain, supporting long-term functionality in dynamic body conditions. At the device architecture level, Lee et al. introduced an f-MDPE synaptic array featuring a simplified vertical stacking design that eliminates the need for selector components and reduces operational voltages (Figure 5A).[134] This approach not only enhances fabrication scalability but also preserves high classification accuracy on flexible substrates, making it highly suitable for integration into epidermal electronics. Building upon these advancements in flexibility and integration, a recent study by Cao et al. exemplifies how such technologies are being translated into implantable systems. They developed a polydimethylsiloxane-encapsulated $Ag/MnO_2/BaTiO_3/FTO$ memristor specifically designed for real-time pulmonary artery pressure monitoring. Uniquely, this device demonstrated both excellent *in vivo* biocompatibility and stable synaptic behavior over a 4-week implantation in SD rats.[139] Together, these developments illustrate a growing convergence between neural adaptability and soft-material engineering. By embedding synaptic behavior into stretchable, conformal frameworks, memristive platforms are evolving into intelligent, body-integrated biosignal processors. This shift supports the realization of neuromorphic devices that do not merely attach to the body, but intimately sense, learn, and adapt to it in real time, marking a pivotal step toward autonomous, self-learning bioelectronic systems for long-term healthcare monitoring and neuroprosthetics.

Neural interfaces

Memristive-based neural interfaces are redefining how artificial systems interact with biological tissues by enabling

energy-efficient, low-voltage, and biocompatible signal integration (Figure 5B). Unlike traditional hardware that operates at high voltages and separates sensing from processing, these neuromorphic platforms integrate synaptic functionality directly into compact architectures, enabling seamless bidirectional communication. Fu et al. demonstrated memristors based on *Geobacter sulfurreducens* protein nanowires that operate at 40–100 mV, which is comparable to natural neuronal action potentials.[140] These devices exhibited dynamic conductance modulation and temporal integration, supporting native-like spike behavior without external regulation circuitry. At the computational level, Tzouvadaki et al. showed that single memristors can detect, sort, and classify spikes directly, functioning as analog processors and eliminating the need for complex preprocessing.[39] This streamlined architecture is ideal for closed-loop brain-machine interfaces (BMIs), where latency and power constraints are critical. For adaptive communication, Serb et al. constructed synaptic ''synaptor'' links between silicon-based spiking neurons and live hippocampal cultures using TiOx memristors.[135] These devices emulate Hebbian plasticity by adjusting synaptic weight in response to spiking activity, supporting both long-term potentiation and depression, which is key for learning and adaptation in bioelectronic systems. Furthering this vision, Shchanikov et al. developed a hybrid neural platform combining crossbar arrays, deep neural networks, and cultured neurons (Figure 5C).[141] Their system adjusts stimulation patterns dynamically based on biological feedback, ensuring robustness against signal degradation. This architecture exemplifies how real-time, intelligent neuroprosthetics can maintain functional stability over time. The combined findings indicate that memristive platforms offer capabilities extending beyond simple signal transmission to full biological-grade information processing. By co-locating sensing, adaptation, and memory in compact architectures, memristive neural interfaces offer a powerful route toward seamless integration between nervous systems and electronics.

Edge intelligence

Edge intelligence is experiencing a paradigm shift through memory-based neuromorphic computing platforms capable of performing real-time computation, learning, and security operations at the data generation point, eliminating dependence on centralized servers. This *in situ* capability is particularly critical for IoMT applications, where latency, bandwidth, and data privacy are major constraints. Zhao et al. developed a memristive image reconstructor (MIR) that executes discrete Fourier transforms entirely in memory for computed tomography (CT) and MRI image recovery, as shown in Figure 6A.[142] Using quasi-analog mapping and complex matrix transfer, MIR achieves software-equivalent image quality with 153× energy efficiency and 79× reconstruction speedup over GPU implementations, illustrating the feasibility of high-throughput medical imaging on edge hardware. Addressing diagnostic generalization, Wang et al. proposed a fully integrated memristor-CMOS system-on-chip (SoC) for simultaneous detection of liver cancer and myocardial infarction.[143] The device integrates enhanced Raman signal acquisition with diffusion-model-based data augmentation to achieve 91.82% classification accuracy and sub-second latency, all processed in-memory. With its compact architecture and ultra-low energy footprint, this platform enables multidisease inference in portable or wearable formats. Similarly, Fu et al. demonstrated a memristor-based approach for real-time identification of brain tumor cell malignancy using an Ag/WO_3/Ti device. By detecting resistance changes induced by different glioma cell types, the system enables rapid, label-free diagnostics with high sensitivity.[144] For data confidentiality in decentralized environments, Lai and Wang introduced a 4D memristive hyperchaotic encryption framework using a novel chaotic map based on a discrete memristor (Figure 6B).[145] By incorporating reflection scrambling and split diffusion, their system achieved high entropy (number of pixels change rate >99.6%) and rapid encryption speeds (~30 ms for a 224 × 224 pixel), providing robust, lightweight security suitable for resource-constrained IoMT nodes. In a similar effort to enhance both data security and device sustainability at the edge, Lin et al. proposed a hardware encryption and image reconstruction platform based on a biomemristor fabricated from natural mugwort extract. Their Ag/mugwort:polyvinylidene fluoride (PVDF)/ITO device exhibited reliable resistive switching and unidirectional conduction properties, which enabled the construction of logic gate circuits and a decoder-based encryption module. This allowed unified, in-memory encryption and decryption of both American Standard Code for Information Interchange-coded medical data and grayscale medical images using the same rule set. With a charge transport mechanism governed by Fowler-Nordheim tunneling, redox reactions, and coordination complex formation, the biomemristor-based circuit achieved efficient edge-level processing with environmentally friendly materials.[146] These examples collectively underscore the capacity of memristive neuromorphic systems to handle sensing, inference, and encryption on a single chip, fundamentally transforming the edge computing paradigm. By embedding computation into memory and leveraging native stochasticity and non-linearity, memristive platforms enable real-time, secure, and energy-proportional decision-making in medical systems deployed far from the cloud.

Toward integrated systems

Recent progress in memristive neuromorphic technologies has moved beyond isolated device demonstrations toward more cohesive system-level implementations. Increasingly, biosignal processors, neural interfaces, flexible substrates, and secure edge intelligence are being designed, not as standalone modules, but as interlinked components of integrated bioedge systems. Early prototypes now co-locate sensing, memory, and computing within single platforms, enabling closed-loop operation in wearable and implantable formats. Some systems combine real-time classification with feedback stimulation, while others integrate encryption or multimodal signal fusion directly in hardware. These developments mark a shift toward compact, adaptive microsystems that perform personalized analysis and actuation near or within the body. While full integration is still emerging, these trends illustrate a growing convergence across materials, device architectures, and edge-AI models. Together, they form the technical foundation for next-generation bioelectronic systems that are autonomous, efficient, and increasingly aligned with the physiological complexity of real-world healthcare settings.

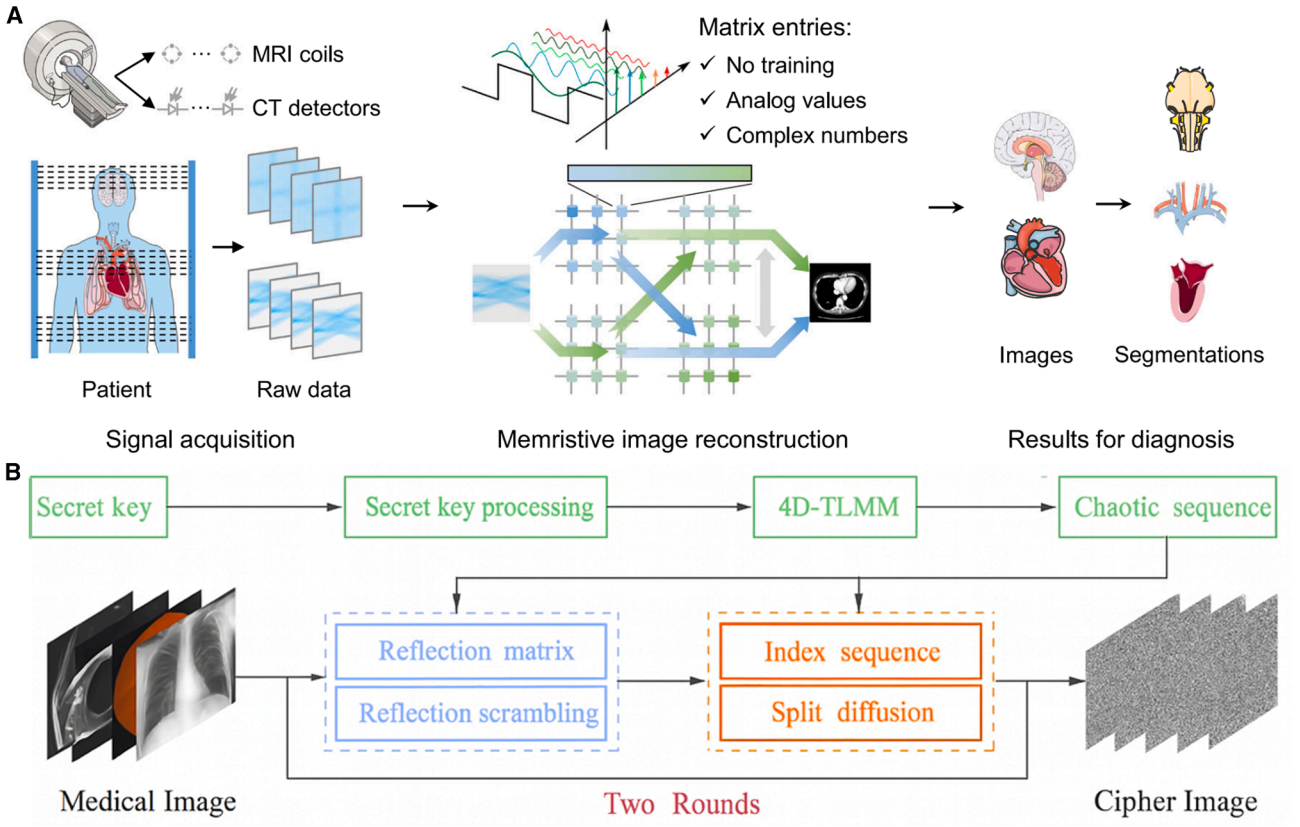

Figure 6. Schematic illustration of memristor-enabled medical-image reconstruction and secure encryption

(A) End-to-end pipeline for tomographic image formation accelerated by memristive crossbar hardware. Raw *k*-space (MRI) or projection (CT) signals are first acquired by multiple receiver coils or X-ray detectors. The data are then streamed into an analog crossbar array whose conductance matrix stores the inverse imaging operator directly—no iterative training, fully complex, and continuous valued. Single-pass vector-matrix multiplication reconstructs the volumetric image, which is subsequently passed to AI segmentation algorithms for organ-specific diagnosis (brain, heart, vasculature, or valve). Reproduced with permission.[143] Copyright 2023, Nature.

(B) Schematic of the transmission line matrix method–iterative equivalent algorithm (TLMM-IEA) encryption scheme for medical image protection in IoMT. A 256-bit secret key initializes the 4D memristive hyperchaotic map (4D-TLMM) to generate a high-entropy chaotic sequence. The encryption process includes reflection scrambling to disrupt pixel positions and split diffusion to spread pixel values globally. Reproduced with permission.[145] Copyright 2024, Springer.

CHALLENGES AND FUTURE OF NEUROMORPHIC IoMT

Challenges

From a device-level perspective, although RRAM, FeRAM, MRAM, and photonic memories each exhibit specific strengths, such as low power consumption, long retention, high endurance, or fast switching speeds, no single technology currently fulfills all the stringent demands of IoMT applications. Furthermore, fabrication processes for these devices continue to face critical challenges, including device variability, limited yield, and long-term reliability. When deployed in crossbar arrays for analog in-memory computing, such non-idealities, particularly variation and aging, can degrade the accuracy of weight mapping. Additionally, circuit-level issues such as IR drop and sneak path currents further compromise the fidelity of matrix-vector multiplication, thereby affecting the performance of neuromorphic neural networks. While some training frameworks have accounted for individual hardware non-idealities to mitigate accuracy degradation, a comprehensive and standardized framework that simultaneously addresses aging, stuck-at faults, variability, IR drop, and sneak paths remains lacking (Figure 7E). This significantly hinders the reliable deployment of neuromorphic hardware in critical biomedical and IoMT scenarios, where precision, stability, and energy efficiency are paramount.

From an integration standpoint, emerging memory materials such as perovskites and 2D materials offer exciting opportunities, yet their poor compatibility with standard CMOS processes remains a major obstacle to practical adoption (Figure 7D). By contrast, ferroelectric memories, particularly those based on hafnium oxide, have gained significant attention due to their inherent compatibility with established CMOS fabrication technologies. Beyond materials integration, developing robust and scalable in-memory computing architectures presents further challenges. Although crossbar arrays can efficiently accelerate matrix-vector multiplications in neural networks using analog

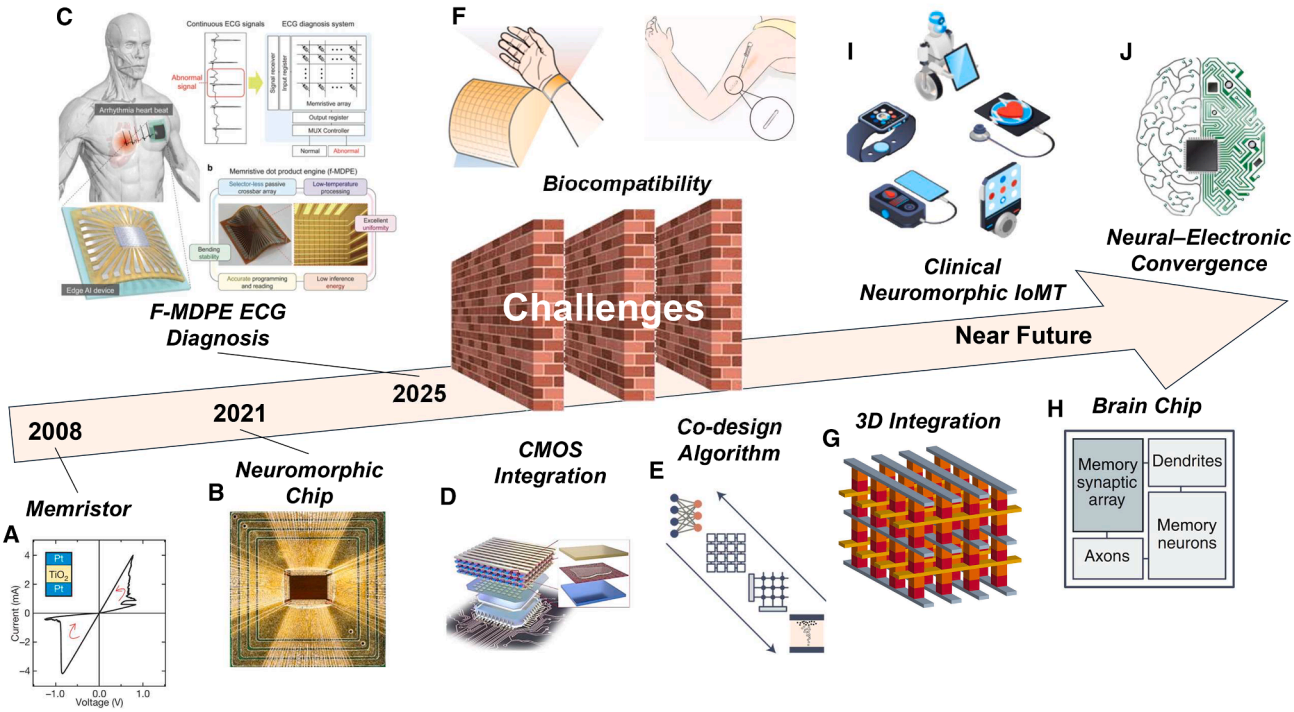

Figure 7. Roadmap and future perspectives for the neuromorphic Internet of Medical Things from memory-device-level innovations to brain-inspired neuromorphic clinical systems

This figure presents the technological and clinical evolution of the neuromorphic IoMT, mapping out key milestones from device-level innovations to envisioned clinical applications.

(A–C) Starting with (A), the introduction of the memristor, reproduced with permission,[41] copyright 2008, Nature; (B) the roadmap includes the development of f-MDPE-ECG diagnostic devices, reproduced with permission,[134] copyright 2025, Nature; and (C) Early neuromorphic chips, reproduced with permission,[147] copyright 2021, Nature.

(D–F) Major challenges, including (D) CMOS and system integration, reproduced with permission,[148] copyright 2024, Nature; (E) co-design algorithms bridging hardware and neural models, reproduced with permission,[13] copyright 2020, Nature; and (F) biocompatibility, reproduced with permission,[134] copyright 2025, Nature, are on the path to near-future clinical deployment.

(G–J) The future trends and opportunities include the (G) highly efficient 3D integration architectures, reproduced with permission,[13] copyright 2020, Nature; (H) highly integrated brain-inspired chips, reproduced with permission,[13] copyright 2020, Nature; (I) intelligent clinical neuromorphic IoMT systems for real-time health monitoring; and (J) neural-electronic convergence through highly integrated brain-inspired chips.

computation, their outputs must be digitized using ADCs, which typically consume much more power than the crossbars themselves. While sharing ADCs across multiple crossbars can reduce hardware overhead, this strategy compromises throughput and computational efficiency. In near-sensor or in-sensor computing paradigms, co-integrating sensors, emerging memory devices, and CMOS circuits onto a single chip further complicates system design and fabrication. Designers must not only address integration and layout challenges but also compensate for sensor non-idealities such as drift, noise, and non-linearity. These co-design and integration hurdles remain key bottlenecks in the realization of compact, energy-efficient, and multifunctional neuromorphic systems for biomedical and IoMT applications.

From a biomedical application perspective, external IoT devices typically emphasize constraints on power consumption and device miniaturization. However, more advanced scenarios, such as ingestible electronics and subcutaneously implanted devices, impose significantly harsher environmental requirements. In such *in vivo* applications, memory devices must maintain stable operation despite fluctuations in pH, humidity, and mechanical stress. Long-term functional reliability under these conditions is essential. Additionally, biocompatibility becomes a critical design criterion: all materials used in implantable electronics must be non-toxic, non-inflammatory, and safe for prolonged interaction with biological tissues (Figure 7F). For memory devices, this translates to rigorous requirements for mechanical flexibility and structural robustness; they must retain endurance, retention time, and fault tolerance (e.g., avoid stuck-at faults) even after repeated bending and deformation. These characteristics are essential to ensure seamless integration onto flexible printed circuit boards or bioresorbable substrates, as commonly required in soft and implantable biomedical electronics.

Future of the neuromorphic IoMT

The future of neuromorphic computing within the IoMT presents promising prospects driven by breakthroughs in materials science, brain-inspired computational architectures, and integrated bioelectronic systems. This multidisciplinary convergence will

significantly enhance healthcare technologies, facilitating more intuitive, responsive, and biologically integrated medical applications. The development roadmap and future work trend for the neuromorphic IoMT is shown in Figure 7.

Advancements in novel memory materials will play a foundational role in the evolution of neuromorphic IoMT devices. Two-dimensional materials, perovskites, and ferroelectric HfO_2 are poised to revolutionize device performance, achieving exceptional energy efficiency, rapid switching speeds, and prolonged endurance. Precise atomic-scale control will mitigate device variability, enhancing reliability crucial for biomedical applications. Hybrid materials combining organic flexibility with inorganic robustness will offer superior mechanical adaptability, enabling seamless integration into wearable, implantable, or even bioresorbable medical systems. Such material innovations will be instrumental in realizing compact, long-lasting, and biologically compatible neuromorphic technologies suitable for diverse clinical scenarios.

The transition from conventional von Neumann architectures to genuine brain-inspired computational systems, encompassing both hardware architectures and bioinspired algorithms, will be transformative. Future emerging memory-based neuromorphic chips will integrate crossbar arrays utilizing advanced selector devices, three-dimensional stacking, and optimized routing strategies to overcome traditional challenges like sneak-path currents and IR drop (Figure 7G). Simultaneously, bioinspired computational models such as SNNs, reservoir computing, and neuromorphic transformer architectures will enable real-time adaptive learning and processing capabilities. On-chip implementations of STDP, unsupervised learning methods, and hybrid neural architectures combining analog and digital computation will foster highly adaptive, resilient, and energy-efficient medical devices (Figure 7H). These innovations will significantly enhance the autonomy and precision of IoMT applications, driving toward real-world implementations of intelligent, adaptive healthcare systems.

The future of the neuromorphic IoMT will increasingly emphasize sophisticated biointegrated systems and their transformative clinical potential. Clinical applications will encompass real-time cardiac anomaly detection, adaptive neural interfaces for neuroprosthetics, personalized therapeutic modulation systems, and intelligent implantable drug delivery platforms (Figure 7I). Furthermore, autonomous, self-powered systems utilizing bioinspired energy harvesting technologies, such as triboelectric nanogenerators or enzymatic biofuel cells, will further extend device lifetimes and reduce clinical maintenance requirements. Enhanced neuromorphic platforms will be deeply integrated into flexible and stretchable bioelectronics capable of conforming seamlessly to biological tissues, thus enabling continuous, non-invasive physiological monitoring and intervention (Figure 7J). These integrated bioelectronic systems will pave the way for revolutionary medical paradigms characterized by personalized, continuous, and proactive healthcare delivery.

Looking forward, advancements in emerging memory material innovations, genuinely brain-inspired computational architectures, and highly integrated bioelectronic systems will define the future of the neuromorphic IoMT. This interdisciplinary synergy among materials science, computational neuroscience, bioelectronics, and clinical medicine will foster the development of robust, intelligent medical devices, ultimately transforming patient care toward unprecedented levels of integration, personalization, and clinical effectiveness.

ACKNOWLEDGMENTS

The authors acknowledge support from the Nanyang Assistant Professorship Start-up Grant and the Eric and Wendy Schmidt AI in Science Postdoctoral Fellowship, a Schmidt Futures program.

AUTHOR CONTRIBUTIONS

Conceptualization, T.C. and H.-W.H.; literature search and data curation, T.C., C.S., D.W., and H.Z.; visualization, T.C., C.S., and D.W.; writing – original draft, T.C., C.S., and D.W.; writing – review & editing, T.C., C.S., D.W., H.Z., R.T., Z. Z., H.L., B.L., and M.Z.; supervision, T.C. and H.-W.H.; funding acquisition, H.-W.H.

DECLARATION OF INTERESTS

All authors declare no competing interests.

DECLARATION OF GENERATIVE AI AND AI-ASSISTED TECHNOLOGIES IN THE WRITING PROCESS

During the preparation of this work, the authors used OpenAI GPT-4o to assist with grammar correction. After using this tool, the authors thoroughly reviewed and edited the content as needed and take full responsibility for the final version of the manuscript.

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